REMARKS

Claims 1-12 are pending in the application. Claims 1-2, 4, 6 and 8-12 are rejected. Dependent claims 3, 5 and 7 are objected to as being dependent on a rejected base claim but would be allowable if rewritten into independent form.

The most recent Office Action rejects the claims for the same reasons that were presented in a previous office action and it explains why Applicants' response to the previous office action was not persuasive. Applicants respectfully maintain the arguments from their previous response and provide reasons below why the explanations given in the most recent Office Action are either not correct or are not pertinent.

Claims 1-10

Claims 1-2, 4, 6 and 8-10 are rejected under 35 U.S.C. § 103 as being unpatentable over U.S. patent 6,031,386 (referred to as "Cole") in view of Acuna et al., "Simulation Techniques for Mixed Analog/Digital Circuits," IEEE J. of Solid-State Circuits, April 1990, vol. 25, no. 2, pp. 353-363 (referred to as "Acuna").

Referring to claim 1, the Office Action indicates Cole teaches all that is claimed except that "Cole does not expressly teach that the numerical modeling that is performed is a 'logic simulation' as opposed to a 'transition simulation'"; that Acuna teaches a simulator that performs four types of circuit simulation; and that it would have been obvious to combine the teachings in Acuna with the teachings in Cole to reach the invention as claimed.

Applicants respectfully disagree and traverse the rejection of claim 1 because Cole and Acuna, either alone or in combination, do not disclose or suggest all limitations of claim 1.

Claim 1 reads as follows (letters are added to the claim elements for convenient reference in the following discussion):

> 1. A fault simulation method for a semiconductor IC, said method comprising the steps of:
>
> (a) generating a test pattern sequence composed of two or more test patterns for input to said semiconductor IC;
>
> (b) performing a logic simulation of the operation of said semiconductor IC in the case of applying thereto each of said two or more test patterns of said test pattern sequence, and calculating a logic signal value sequence in each signal line in said semiconductor IC; and
>
> (c) generating a list of faults, which are detectable by a transient power supply current testing using said test pattern sequence, through the use of said logic signal value sequence in said each signal line calculated by said logic simulation.

Cole teaches methods for testing an actual integrated circuit (IC) that either measures the transient component of the IC operating voltage (see col. 3, lns. 33-39) or the time delay of the transient component of the operating voltage (col. 3, lns. 47-52). Reference values that may be used to determine if a measured component is out of bounds, thereby indicating a failure exists in the IC, may be obtained by measuring known good ICs or by numerical modeling (col. 3, lns. 42-45 and 59-62). Acuna teaches methods for circuit simulation, which can be used for the numerical modeling mentioned in Cole.

As explained in their previous response, the method of claim 1 is not directed toward testing an actual semiconductor IC *per se*. Claim 1 recites steps of a method for generating a list of faults in a semiconductor IC that are capable of being detected by transient power supply current (TPSC) testing. The method of claim 1 does not actually test an IC but instead produces a list of faults that may be used to design a set of test patterns for more efficient testing of an actual IC.

The Office Action indicates element (b) of claim 1 "corresponds to a form of testing semiconductor ICs due to the 'applying' of 'test patterns' to the circuit." Applicants disagree and respectfully submit there is no known prior art that supports this assertion. Although logic simulation may be used to test the correctness of an IC **design**, it does not test an actual IC.

Applicants also explained in their previous response that neither Cole nor Acuna disclose or suggest anything pertinent to determining which faults are capable of being detected by TPSC testing. Cole tacitly admits its disclosed method of testing, as well as other known methods of testing, are incapable of detecting all kinds of faults. In particular, Cole states the following:

> Pinpointing of different types of defects and failure mechanisms in an IC generally requires the use of different analytical methods, since each analytical method has certain advantages and disadvantages (col. 1, lns 26-29).

Although Cole indicates not all types of faults can be detected by a given method of testing, Cole does not teach anything that allows a person of ordinary skill in the art to determine which faults are capable of being detected by its disclosed methods of testing or by any other methods of testing.

The Office Action indicates Applicants' statement is not correct by asserting Cole does teach how to determine which faults are detectable as shown by the following:

> The transient voltage component V_{DDT} is used to provide an indication of any defects present within each IC 100 being tested by the apparatus 10, and in particular defects that alter an electrical current to the IC 100. (col. 4, lns 59-64, emphasis added by Examiner).

This teaching in Cole is not relevant to the invention as claimed. It merely explains that the testing techniques disclosed in Cole are capable of detecting defects that alter an electrical current

supplied to the IC. This goes without saying. A testing technique that measures only a signal that is external to an IC cannot detect a defect in the IC that does not alter this signal in some way. Even if this statement was relevant, it does not teach or suggest any technique for determining whether a particular defect is detectable by the recited testing method. In other words, Cole does not teach how to determine whether a particular fault will "alter an electric current to the IC 100" and, therefore, determine whether the fault is capable of being detected.

The Office Action also quotes the following from Cole:

> In using the present invention, it is generally not desirable to individually test every transistor gate in the IC 100 for defects or failure mechanisms. This is especially the case in a production environment where the goal is to qualify large numbers of ICs as being substantially free of defects or failure mechanisms, while minimizing the time required for testing. The set of test vectors can be determined from the design of a particular IC 100, and an exact set of test vectors can vary depending on whether the apparatus 10 is to be used for production testing, or for failure analysis.

The text quoted from Cole is not pertinent to the claimed invention. Cole merely teaches that a set of vectors for testing some representative subset of the transistors can be determined from the design of the particular IC to be tested. In other words, after choosing some representative subset of transistors for testing, the design of the IC can be consulted to determine a set of vectors to test the chosen transistors. It is significant to note that there is nothing in the quoted text or in any other part of Cole that teaches how to determine whether a particular fault is capable of being detected. For example, Cole does not teach how to determine whether a delay fault of e.g. 0.1 ns can be detected, whether multiple stuck-at-zero faults can be detected, or whether open faults as opposed to short faults can be detected.

Cole in view of Acuna does not disclose or suggest what is claimed: (1) performing logic simulation to calculate a logic signal value sequence, and (2) using the logic value sequence to generate a list of faults that are capable of being detected by the TPSC testing method.

Similar reasons apply to claim 10. Claims 2-9 depend on claim 1 and add further limitations.

Applicants do not find anything in Cole or Acuna that suggests the claimed list of detectable faults or any means for generating it, and they find no suggestion for TPSC testing. If the rejection of claims 1, 2, 4, 6 and 8-10 is to be maintained, Applicants request that the next communication explain where the TPSC testing method is disclosed or suggested, what feature is the claimed list of detectable faults and what feature is believed to generate this list.

Claims 11-12

Claims 11-12 are rejected under 35 U.S.C. § 103 as being unpatentable over Cole in view of Carmichael et al., "Simulation as an aid to power supply diagnostics," Conf. Record of AUTOTESTCON '95, Atlanta, Aug. 8-10, 1995, pp. 556-56 (referred to as "Carmichael").

The Office Action indicates Cole teaches all that is claimed except for specifically mentioned limitations that pertain to inserting an assumed fault in a semiconductor IC and deciding whether the assumed fault is detectable; that this missing teaching is provided by Carmichael; and that it would have been obvious to combine teachings from Cole and Carmichael to reach the invention as claimed.

Applicants respectfully disagree and traverse the rejection of claims 11-12 because Cole and Carmichael, either alone or in combination, do not disclose or suggest all limitations of the claims. Neither Cole nor Carmichael teach how to determine which faults are detectable by transient power supply current (TPSC) testing. Neither reference discloses or even suggests the TPSC testing method. Carmichael does disclose circuit simulation of a power supply but this is not the same as TPSC testing that monitors the transient nature of the power supply current to another device.

The previous office action and the most recent Office Action both state that "Cole does not expressly teach ... deciding whether the assumed fault is detectable, or generating a fault list in which the detectable faults are registered." In their previous reply, Applicants explained that Carmichael also does not teach this feature.

As explained previously, Carmichael discusses research in which engineers simulated operation of a power supply circuit with a numerical model and used this model as an aid to determine manually how several assumed faults affected circuit operation. There is no suggestion for any technique that determines whether a particular fault can be detected by TPSC testing.

The Office Action indicates Applicants' previous reply was not adequate because one cannot show nonobviousness over a combination of references by attacking references individually. In this instance, however, Applicants' arguments against the Carmichael reference were sufficient because the previous office action admitted Cole, the only other reference used in the combination, did not disclose the feature that Applicants explained was also not taught in Carmichael.

Applicants do not find anything in Cole or Carmichael that suggests the claimed list of detectable faults or any means for generating it, and they find no suggestion for TPSC testing. If the rejection of claims 11-12 is to be maintained, Applicants request that the next communication explain where these features are disclosed or suggested.

CONCLUSION

Applicants request reconsideration of the claims in view of the discussion set forth above.

Respectfully submitted,

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Certificate of Transmission

I certify that this Response to Office Action and any following materials are being transmitted by facsimile on February 3, 2005 to the U.S. Patent and Trademark Office at telephone number (703) 872-9306.

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